TFW

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re the Application of: **TOKUDA, Kazuhiko**

Group Art Unit: **3729**

Serial No.: **09/928,441**

Examiner: **Rick Kiltae Chang**

Filed: **August 14, 2001**

P.T.O. Confirmation No.: 8352

For: **A METHOD OF FORMING WIRING LINES ON A BOARD TO FORM A CIRCUIT BOARD**

Request for Reconsideration under 37 CFR 1.111

MAILSTOP Amendment

Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

May 31, 2006

Sir:

In response to the Office Action dated **March 3, 2006**, Applicant respectfully requests that the Examiner reconsider and remove the rejection of Claims 37 and 38.

Claims 37 and 38 read as follows:

Claim 37. A method of forming a plurality of wiring lines on conductive material on a board having a core layer to form a printed circuit board, comprising:

(a) forming said plurality of wiring lines on a surface of said core layer, having first and second portions, the plurality of wiring lines formed on said surface of said core having side walls of a uniform thickness in height relative to said surface of said core layer; and

(b) etching the first portion of a first of said plurality of wiring lines, such that the first portion has a planar surface completely across said first portion, joining said side walls, and is thinner in height relative to said surface of said core layer than the second portion, such that cross-talk noise between adjacent two wiring lines is reduced , wherein the first portion is parallel to at least one of the plurality of wiring lines other than the first of the plurality of wiring lines.

Claim 38. The method as claimed in claim 37, wherein a second of said plurality of said wiring lines is provided, spaced from said first wiring line of said plurality of wiring lines having said first and second portions, said second wiring line having third and fourth portions, and etching said second wiring line such that the third portion is thinner in height relative to said surface of said core layer than the fourth portion, wherein the third portion is parallel to the first portion.

In the Office Action dated March 3, 2006, Claims 37 and 38 were rejected as anticipated under 35 U.S.C. 102(b) by Gali et al. (U.S. 3,781,596). The Office Action alleges that Gali discloses etching of (71) to form a plurality of wiring lines on a surface of a core layer and further etching (71) using a mask to form a different thickness first portion (12) then a second portion (13), referring to Fig. 1a. Fig. 2 is referred to to show a first portion of one line with (13) parallel with another line (12) other than the one next to (13). Reconsideration and removal of this rejection is respectfully requested in view of the following remarks.

The purpose of applicant's method is to form a plurality of wiring lines on a board in a manner that reduces cross-talk noise between adjacent two wiring lines.

Cross-talk noise depends on the length of a wiring line. By reference to the formula:

$V=Vk \times Td/Tr \quad (Tr \geq 2 \times Td)$

where V denotes a cross-talk voltage [V],

Vk denotes a cross-talk voltage [V] when $2 \times Td \geq Tr$,

Tr denotes a rising time [sec] of a signal, and

Td denotes a propagation time [sec] of the wiring line:

the formula of the cross-talk value is different depending on a rising time of a signal.

This is a simple formula used where a wiring line is short in length. To the contrary, the formula on page 5 of the present specification is for a case where ($2 \times Td \geq Tr$).

The Gali reference makes no reference whatsoever to cross-talk or how to reduce the same. This is because the length of Gali's wiring line is only a few millimeters. As stated at Col. 1, lines 19-21 of Gali et al.; "This invention relates to semiconductor chips, and more specifically, to mounting such chips on substrates." Thus, it is readily apparent that the size of the wiring lines would be in the range of only a few millimeters. With such a short length, cross-talk would not be an issue. In the present method, however, with reference to Fig. 1 of the present specification, by comparing the size of semiconductors 2a, 2b, and 2c with wiring lines among them, portions of the wiring lines in the present invention are longer than the widths of the semiconductors 2a, 2b, and 2c. Accordingly, it is obvious that the length of the wiring lines of the present invention are longer than the length of the wiring lines of Gali and can be recognized to be dozens of millimeters.

As previously mentioned, Gali does not disclose anywhere a problem of cross-talk noise, and this is because his etched portions would be only a few millimeters in length and have a uniform height except for pads (13).

The disclosure of the Gali et al. reference simply does not lead one to the present claimed method of forming a plurality of wiring lines on a board such that cross-talk between adjacent two wiring lines is reduced, and only the teachings of Applicant's specification would lead one to the present method.

If there are any issues of a minor nature remaining, the Examiner is urged to contact Applicant's attorney, the undersigned, at Area Code (202) 659-2930.

Respectfully submitted,

ARMSTRONG, KRATZ, QUINTOS, HANSON & BROOKS, LLP

DARREN R. CREW (REG. NO. 37,806)
for William G. Kratz, Jr.
Attorney for Applicant
Reg. No. 22,631

WGK/bak

Atty. Docket No. **000958A**
Suite 1000,1725 K Street, N.W.
Washington, D.C. 20006
(202) 659-2930

23850
PATENT TRADEMARK OFFICE

H:\HOME\NANCY\00\000958A\Amendment filed 5-31-06